semiconductor substrate is provided with a plurality of semiconductor devices arranged thereon. An interconnect structure, which comprises a plurality of conductive and insulating layers that are formed one over another in alternating fashion, is formed over the substrate to couple semiconductor devices to one another. A conductive lower capacitor electrode layer is formed over the interconnect structure. A co-sputtering process is performed to form a capacitor dielectric over the conductive lower capacitor electrode. A conductive upper capacitor electrode layer is formed over the capacitor dielectric.

Still other embodiments relate to an integrated circuit (IC) device including a metal-insulator-metal (MIM) capacitor structure. The MIM capacitor structure includes a lower TiN capacitor electrode; an upper TiN capacitor electrode; and an amorphous SiO2 capacitor dielectric. The capacitor dielectric has a thickness of less than approximately one hundred Angstroms, and separates the lower TiN electrode from the upper TiN electrode. The capacitor dielectric has a dielectric constant of greater than one-hundred. A plurality of metal or metal oxide/nitride nano-particles, which have individual diameters of less than approximately ten nanometers, are randomly distributed over an entire volume of amorphous SiO2 capacitor dielectric between the upper and lower TiN capacitor electrodes.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method of forming a metal-insulator-metal (MIM) capacitor:

providing a semiconductor substrate with a plurality of semiconductor devices arranged thereon, wherein an interconnect structure, which comprises a plurality of conductive and insulating layers that are formed one over another in alternating fashion, is formed over the semiconductor substrate to couple semiconductor devices to one another;

forming a conductive lower capacitor electrode over the interconnect structure;

performing a co-sputtering process to form a capacitor dielectric over the conductive lower capacitor electrode, wherein performing the co-sputtering process comprises sputtering an elemental material from a target that is a pure element, such that oxide or nitride forms on the conductive lower capacitor electrode from the elemental material; and

forming a conductive upper capacitor electrode over the capacitor dielectric.

2. The method of claim **1**, wherein the co-sputtering process comprises:

arranging the semiconductor substrate on an engagement surface within a vacuum chamber;

while the semiconductor substrate is on the engagement surface, using a first direct current (DC) bias to sputter dielectric material from a dielectric target, which is arranged in the vacuum chamber, onto a surface of the conductive lower capacitor electrode; and

while the dielectric material is being sputtered from the dielectric target, using a second DC bias to concurrently sputter a metal material from a metal target, which is arranged in the vacuum chamber;

wherein the target is the dielectric target or the metal target.

3. The method of claim **1**, wherein the capacitor dielectric is made up of an amorphous oxide or amorphous nitride matrix, and a series of metal or metal oxide or metal nitride nano-particles that are randomly distributed over a volume of the amorphous oxide or amorphous nitride matrix.

4. The method of claim **3**, wherein the metal or metal oxide or metal nitride nano-particles have average diameters ranging between 6 nm and 10 nm.

5. The method of claim **3**, wherein the amorphous oxide or amorphous nitride matrix is made up of amorphous SiO2.

6. The method of claim **3**, wherein the metal or metal oxide or metal nitride nano-particles include Ti, Zr, Hf, or a combination of the foregoing.

7. The method of claim **1**, wherein the capacitor dielectric separates upper and lower electrodes of a resistive random access memory (RRAM) device or separates an anode and cathode of a diode.

8. The method of claim **1**, wherein the elemental material is metal, and wherein the oxide or nitride forms on the conductive lower capacitor electrode as nano-particles of metal oxide or of metal nitride.

9. The method according to claim **8**, wherein performing the co-sputtering process further comprises sputtering a silicon material from a pure silicon target, such that silicon dioxide is deposited on the conductive lower capacitor electrode as a bulk of the capacitor dielectric.

10. A method of forming an integrated circuit (IC), the method comprising:

forming a lower TiN electrode;

forming an amorphous SiO_2 or amorphous Al_2O_3 dielectric, which has a thickness of less than approximately one hundred angstroms and a dielectric constant of greater than twenty, over the lower TiN electrode, wherein a plurality of metal or metal nitride nano-particles, which have individual diameters of less than approximately ten nanometers, are randomly distributed over an entire volume of the amorphous SiO_2 or amorphous Al_2O_3 dielectric; and

forming an upper TiN electrode over the amorphous SiO_2 or amorphous Al_2O_3 dielectric.

11. The method of claim **10**, wherein the metal or metal nitride nano-particles include Ti, Zr, Hr, or a combination of the foregoing.

12. The method of claim **10**, wherein forming the amorphous SiO_2 or amorphous Al_2O_3 dielectric comprises a co-sputtering process wherein a dielectric material and a conductive material are concurrently sputtered from different targets to form the amorphous SiO_2 or amorphous Al_2O_3 dielectric.

13. The method of claim **12**, wherein the co-sputtering process comprises:

using a first direct current (DC) bias to sputter the dielectric material from a dielectric target, which is arranged in a vacuum chamber, onto a surface of the lower TiN electrode; and

while the dielectric material is being sputtered from the dielectric target, using a second DC bias to concurrently sputter conductive nano-particles from a conduc-